

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: LAYOUT TECHNIQUE FOR ADDRESS SIGNAL LINES IN
DECODERS INCLUDING STITCHED BLOCKS

APPLICANT: RICHARD H. TSAI

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL688319756US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit May 16, 2001

Signature

Gildardo Vargas

Typed or Printed Name of Person Signing Certificate

LAYOUT TECHNIQUE FOR ADDRESS SIGNAL LINES IN DECODERS INCLUDING STITCHED BLOCKS

[0001] This application claims priority to U.S. Provisional Application Serial No. 60/204,371, filed on May 16, 2000 and entitled "An Optimal Layout Technique for Row/Column Decoders to Reduce Number of Blocks."

BACKGROUND

[0002] Many semiconductor processing foundries have a maximum lithographic size they may use to form a chip. A common limit, for example, is 20 x 20 mm². Making a chip larger than that maximum size may be carried out using stitching. Stitching forms different portions of the chip in different areas of the wafer. The different areas are then "stitched" together with interconnect lines to form the overall chip.

[0003] Complicated chips may require a large number of stitches to form an entire circuit. The complexity of the chips may increase the cost and defect rate of the chips and lower throughput in the chip production process.

SUMMARY

[0004] A binary decoder block according to an embodiment includes a number N of generic blocks which are stitched together. Each generic decoder block includes a number of address lines for addressing decoders in the generic decoder block, and no more than $2 \cdot (2^k - 1) + N$ block address lines for addressing the generic blocks, where k is the whole number portion of $\log_2(N-1)$.

[0005] A gray decoder block according to an embodiment includes a number N of generic blocks which are stitched together. Each generic decoder block includes a number of address lines for addressing decoders in the generic decoder block, and no more than $2 \cdot (2^k - 1) + 2(N-1)$ block address lines for addressing the generic blocks.

[0006] A decoder block according to an alternate embodiment includes a number N of generic blocks which are stitched together. Each generic decoder block includes a number of address lines for addressing decoders in the generic decoder block, and no more than N block address lines. The decoder block includes a block address decoder for selecting block address lines corresponding to a selected generic block in the decoder block.

[0007] In a sensor including the decoder block and a pixel section, the features in the decoder block may have a

smaller pitch than the features in the pixel section, for example, a ratio of 0.98 or less. The smaller pitch of the decoder block may provide more area on the silicon surface of the chip for the routing liens used to stitch together the component blocks of the decoder block. Interconnects between the decoder block and the pixel section may be angled to accommodate the larger stitching sections.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a schematic diagram of a binary decoder including four stitched generic blocks according to an embodiment.

[0009] Figure 2 is a schematic diagram of a block address line section in a generic block for use in a binary decoder including five stitched blocks according to an embodiment.

[0010] Figure 3 is a schematic diagram of a block address line section in a generic block for use in a gray code decoder including four stitched blocks according to an embodiment.

[0011] Figure 4 is a schematic diagram of a block address line section in a generic block for use in a gray code decoder including five stitched blocks according to an embodiment.

[0012] Figure 5 is a schematic diagram of a block address line section in a generic block for use in a gray code decoder including eight stitched blocks according to an embodiment.

[0013] Figure 6 is a schematic diagram of an interconnect layout for use in a decoder block including stitched blocks according to an embodiment.

[0014] Figure 7 is an enlarged portion of the diagram of Figure 6 illustrating a layout for interconnect lines in the decode block.

DETAILED DESCRIPTION

[0015] The present disclosure describes a layout technique for stitching blocks together to form row and/or column decoders for use in large image sensors. These sensors are often larger than the typical reticle size of 20 x 20 mm². Thus, these sensors may need to be stitched together using several blocks. A decoder block for use in the image sensor may include a number of different blocks stitched together to form the complete decoder block. An exemplary column decoder block 100 may use 1024 column decoders 102 with a 25 μ m pitch, as shown in Figure 1. To accommodate a typical reticle size of 20 x 20 mm², requires that this block be divided into four pieces. According to

an embodiment, instead of using four blocks with different designs, a block with a generic design may be used repeatedly. The use of generic blocks may save area on the reticle and reduce the complexity of the overall design.

[0016] Each generic block 104-107 includes 256 row or column decoders 102, numbered from 0 to 1023 in the decoder block 100. In order to address each decoder 102 individually, each generic block includes address signal lines NB0-B9 capable of generating a 10-bit address for the 1024 decoders. The signals on lines NB0-NB9 are the inverse of signals on lines B0-B9, respectively. The 10-bit addresses of the decoders may be split logically into an 8-bit portion (NB0-B7) to identify the 256 in-block decoder positions, and a 2-bit portion (NB8-B9) to identify the four generic blocks 104-107.

[0017] The block signal lines NB8-B9 are interleaved and such that they switch position between adjacent blocks. The position of lines NB8 and B8 switch between each block. The bottom signal line 120 of the four lines in the NB9/B9 section in a block 104, 105, 106 crosses over the other three lines and switches position to be the top line 122 in the next adjacent block 105, 106, 107, respectively. Also, the NB9 and B9 lines are arranged such that the type of the top signal line 122 in the NB9/B9 section changes in the

sequence NB9, NB9, B9, B9 in generic blocks 201-204. With B9=1 and NB9=0, this sequence is [0011].

[0018] Each decoder 102 in the generic block includes block addressing lines 110 representing the two most significant bits of the decoder's 10-bit address. The address signal lines 112 for each decoder 102 in the generic block are connected to the top signal line in each of the NB8/B8 and NB9/B9 sections, respectively. With the described layout, each of the generic blocks 104-107 has a different block addresses, [00], [10], [01], and [11], respectively.

[0019] The technique may be expanded to accommodate a larger number of generic blocks. Figure 2 illustrates an exemplary decoder block 200 including five generic blocks 202-206 stitched together to provide 1280 decoders. Each decoder has an 11-bit address, including an 8-bit portion to identify the 256 in-block decoder positions, as described above, and a 3-bit portion to identify the generic block position. The block address signal lines 112 include an NB8/B8 section with two address signal lines, an NB9/B9 section with four address signal lines, and an NBa/Ba section, corresponding to the third bit of the block address, with five address signal lines. Address signal lines in NBa/Ba section are arranged such that the type of

the top signal line 220 changes in the sequence [00001111]. Accordingly, in the five block example, the sequence is [00001] from block 202 to block 206.

[0020] The number of signal lines, $S(N)$, required for a given number of blocks, N , may be expressed by the series $S(2)=2$, $S(3)=2+3=5$, $S(4)=2+4=6$, $S(5)=2+4+5=11$, $S(6)=2+4+6=12$, etc., or generically by the following formula:

$$S(N) = 2 \cdot (2^k - 1) + N; \quad k = \lceil \log_2(N-1) \rceil, \text{ where } k \text{ is the}$$
whole number portion of the logarithm.

[0021] Decoder blocks used in very large sensors may use gray code rather than straight binary code. Gray code is an ordering of binary numbers such that only one bit changes from one state to the next. This may avoid errors, since there is no way of guaranteeing that all bits will change simultaneously at the boundary between two encoded values. For example, using straight binary, it would be possible to generate an output of 0111_2 (15_{10}) in going from 1110_2 (7_{10}) to 1000_2 (8_{10}).

[0022] Figure 3 illustrates an exemplary gray code decoder block 300 including four generic blocks 302-305 stitched together. For the gray decoder, signal lines NB7 and B7 switch position between generic blocks. In each generic block 302-305, the address lines of the decoders in

relative positions 0-127 (first half) are connected to NB7, and the address lines of the decoders in relative positions 128-255 (second half) are connected to B7. There are four signal lines in each of the NB8/N8 and NB9/B9 sections.

The sequence of the type of the top signal line 320 in the NB8/N8 section is [0110], and the sequence of the type of the top signal line 330 in the NB9/B9 section is [0011].

[0023] The technique may be expanded to accommodate a larger number of blocks. Figure 4 illustrates an exemplary gray decoder block 400 including five generic blocks 402-406 stitched together to provide 1280 decoders. The NB8/B8 section includes four signal lines, and each of the NB9/B9 and NBa/Ba sections include five signal lines. The number of signal lines, $S(N)$, required for a given number of blocks, N , may be expressed generically by the formula $S(N) = 2 \cdot (2k-1) + 2(N-1)$.

[0024] In an alternate embodiment, a three-bit block address line decoder 502 is used to select the block address line in a gray decoder block 500 with eight stitched generic blocks 504-511, each including 512 decoders, as shown in Figure 5. Only eight signal lines B1 to B8 are needed to address the eight generic blocks 504-511. The technique may be expanded to accommodate a larger number of blocks. The number of signal lines, $S(N)$,

required for a given number of blocks, N , may be expressed generically by the formula $S(N)=N$.

[0025] For the gray decoder, signal lines A8b and A8 are switched between adjacent generic blocks. For a straight binary decoder, A8b and A8 are not switched.

[0026] To provide more area for the stitching routing lines between generic decoder blocks, a smaller pitch may be applied to the decoder array than the pixel pitch.

Figure 6 illustrates a decoder array 600 for use in a sensor with a $9\text{ }\mu\text{m}$ pixel pitch, where the pitch of the decoder array is reduced to $8.75\text{ }\mu\text{m}$. In a sensor including thirty-two generic blocks, this provides an additional $8\text{ }\mu\text{m}$ of additional silicon space in which to providing the routing lines. Figure 7 illustrates a layout for the angled connection 602 between the decoder array and the pixel array in order to minimize the distance (y_2-y_1) .

[0027] A number of embodiments have been described.

Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.